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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAM, HAI CHI	
ART UNIT	**PAPER NUMBER**
2861	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	09/873,256	EMA ET AL.	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-25 and 27-44* is/are rejected.

7)☒ Claim(s) *13 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *various*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. The following claims are objected to because of the following informalities:

- laim 3:
- Line 8, "high-frequency clock generation means" should read --high-frequency clock generation circuit-- to keep the consistency of the claimed terminologies.
- Line 12, "modulation pattern generation means" should read --modulation pattern generation circuit-- to keep the consistency of the claimed terminologies.
- laim 4:
- Line 8, "high-frequency clock generator" should read --high-frequency clock generation circuit-- to keep the consistency of the claimed terminologies.
- laim 5:
- Line 8, "high-frequency clock dividing means" should read --high-frequency clock divider--.
- laim 38:
- Claim 38 should claim dependency from claim 37 instead of 26. The informality is considered as a typographical error.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-4, 7, 9-12, 14-17, 20-25, 27-28, 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogasawara et al. (U.S. 6,154,246).

Ogasawara et al. discloses an image forming apparatus (Fig. 8) comprising a semiconductor laser (80), an optical unit (85), which scans a rotational photo conductor (drum 90) by a laser light output by said semiconductor laser, and a photodetector (92), which detects the laser light output by said semiconductor laser at a predetermined position, wherein a latent image is formed by scanning said rotational photo conductor based on the laser light detected by the photodetector, said image forming apparatus further comprising a high-frequency clock generation circuit (crystal oscillating circuit 31), a first frequency divider (half frequency dividing circuit 35), which generates and outputs an image clock (image processing clock PCLK), which synchronized with an output of said photodetector (BD signal) by dividing a clock output from the high-frequency clock generation circuit, and an image clock phase changing circuit (BD synchronization circuit 65), which changes a phase of the image clock (col. . 7, lines 59-65).

Regarding claims 27, 34, Ogasawara et al. discloses an image forming apparatus comprising an optical scanning unit (polygon mirror 85) which scans a plurality of light

fluxes on a medium to be scanned (photosensitive drum 90), the light fluxes (80) being synchronous with an output pixel clock (image processing clock PCLK) and being modulated in accordance with image data of a respective one of a plurality of lines, and a clock phase control circuit which controls a phase of said output pixel clock for each of said lines so as to correct a shift in a write start position in a scanning direction due to a shift in a position of each light-emitting point of said plurality of light fluxes (col. 7, lines 59-65).

Osgawara et al. further teaches:

- said high-frequency clock generation circuit comprises a voltage controlled oscillator (VCO 32), which controls an oscillation frequency of a clock, which is output according to an input signal, a second frequency divider (half quarter frequency dividing pre-scaler 34), which divides the clock oscillated by the voltage controlled oscillator, a phase comparator (33), which compares a phase of the clock output by the frequency divider with a phase of a frequency of a reference clock (of frequency fr) so as to output a signal corresponding to a result of the comparison, wherein the signal output by the phase comparator is input to said voltage controlled oscillator (Fig. 6),
- an image data input circuit (not shown), which inputs image data (VDO) based on said image clock, a modulation pattern generation circuit (38), which generates a modulation pattern (image modulating signal PVDO) based on said image data and the clock output from said high-frequency clock generation circuit, and a semiconductor laser control circuit (laser drive circuit 81), which controls the output of said semiconductor laser based on the modulation pattern generated by the modulation pattern generation circuit,

- said first frequency divider, said image clock phase change circuit, said high-frequency clock generating circuit, said image data input circuit and said modulation pattern generation circuit are constituted by an integrated circuit formed in a single semiconductor chip (IC 11) (Fig. 1),
- a frequency dividing operation stop and resumption circuit which stops or resumes an operation of said second frequency divider (using the reset signal generating circuit 16) (Fig. 1) (col. 6, lines 32-45),
- a semiconductor laser turn-off circuit which switches off said semiconductor laser at a timing which delays the phase of said pixel clock (using the reset signal generating circuit 16) (Fig. 1) (col. 6, lines 32-45),
- said phase change circuit changes the timing for taking the image data and the phase of said image clock for every scanning timing (e.g., for every scanning line) (col. 6, lines 40-43),
- said phase change circuit changes the timing for taking the image data and the phase of said image clock only at a first line of a page (inclusive to the above-mentioned scanning timing for each scanning line),
- the clock phase control circuit comprising a second frequency divider (quarter frequency dividing circuit 36), which generates an internal clock by dividing an output of said high-frequency clock generator, the second frequency divider having a circuit which can change a phase of said internal clock.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 18, 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogasawara et al. in view of Ishida et al. (U.S. 6,498,617).

Ogasawara et al. discloses all the basic limitations of the claimed invention except for the frequency dividing ratio setting circuit and the programmable counter.

Ishida et al. discloses an image forming apparatus including a clock generator having a PLL circuit having a programmable divider (59) (Fig. 16), which is also a frequency dividing ratio, which can be arbitrarily set/change by a user (col. 21, lines 51-65).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the frequency dividing ratio setting circuit or programmable frequency divider in the PLL circuit of Ogasawara et al. as taught by Ishida et al. The motivation for doing so would have been to accurately lock the phase of the reference clock generating circuit.

7. Claims 6, 8, 19, 36-37, 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogasawara et al. in view of Swanberg (U.S. 4,694,156).

Ogasawara et al. discloses all the basic limitations of the claimed invention except for the pulse reversal circuit which reverses or forwards a phase of pulses oscillated by said voltage controlled oscillator, and the clock phase control circuit controlling a phase of said output pixel clock to correct a fluctuation in a scanning length.

Swanberg discloses an image forming apparatus comprising a pixel placement control for correcting a fluctuation in the scanning length corresponding to each of the facet of the polygon mirror wherein the phase control corrects a phase lag or a phase change according with the spot velocity and the pixel clock frequency (col. 7, lines 8-31).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the correction of the phase lag or advance in the device of Ogasawara et al. as taught by Swanberg. The motivation for doing so would have been to ensure that every scanning line in a page has the same length.

8. Claims 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogasawara et al. in view of Swanberg, as applied to claims 36-37 above, and further in view of Ishida et al. (U.S. 6,498,617).

Ogasawara et al., as modified, discloses all the basic limitations of the claimed invention except for the programmable counter.

Ishida et al. discloses an image forming apparatus including a clock generator having a PLL circuit having a programmable divider (59) (Fig. 16), which is also a frequency dividing ratio, which can be arbitrarily set/change by a user (col. 21, lines 51-65).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the frequency dividing ratio setting circuit or programmable frequency divider in the PLL circuit of Ogasawara et al. as taught by Ishida et al. The motivation for doing so would have been to accurately lock the phase of the reference clock generating circuit.

Allowable Subject Matter

9. Claims 13 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the primary reason for the indication of the allowability of claims 13 and 26 is the inclusion therein, in combination as currently claimed, of the limitation "the phase of said image clock is changed when being output, and the timing which said image data input circuit takes in data and a timing which said modulation pattern generating circuit generates a modulation pattern are not changed", which is not found taught by the prior art of record considered alone or in combination.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (571) 272-1934. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HAI PHAM
PRIMARY EXAMINER
May 2, 2005